35 U.S.C. § 112

In the February 01, 2000 Office Action, claims 24-27 were rejected under 35 U.S.C. § 112, second paragraph. From item 3 of the February 01, 2000 Office Action "It is not clear from the specification if this list is automatically generated, or if this list is generated manually as the code is modified by the insertion of the instrumentation logic." Applicant respectfully submits that the claims are read in light of knowledge of those skilled in the art. People skilled in the art of writing HDL code know that at the time the HDL code is read by a simulator, the sensitivity list (and therefore the signals therein) of the process is preexisting and is not therefore generated. In the example of figure 18 these signals would be A, B and C of process P1. Process P1 being a preexisting process. Therefore applicant respectfully submits claims 24-27 comply with 35 U.S.C. 112, second paragraph.

35 U.S.C. §102(b)

In the February 01, 2000 Office Action, claims 1-14, 16-18, 20, 22-25, and 28-33 were rejected under 35 U.S.C. § 102(b) as being anticipated by Chen et al. ("A Source-Level Dynamic Analysis Methodology and Tool for High-Level Synthesis", Proceedings of the Tenth International Symposium on System Synthesis, 1997, pp. 134-140, September, hereinafter the Chen et al. reference). Applicant respectfully points out that the reference is dated 17-19 Sept. 1997, less than 1 year from application date, and therefore not proper subject matter for a 35 U.S.C. 102(b) rejection. Nevertheless, as discussed below in the interest of expediting the application process, Applicant respectfully submits that claims 1-14, 16-18, 20, 22-25, and 28-33, as amended, are not anticipated by Chen et al.

Claims 1-14, 16-18, 20, 22, 23, and 28-33

In the February 01, 2000 Office Action, claim 1 was rejected as being unpatentable over a reference to Chen et al. In response, Applicant has amended the claims to clearly distinguish over the cited references.

Amended claim 1 includes:

> A method comprising the steps of:
> a) identifying at least one statement within a register transfer level (RTL) synthesizable source code; and
> b) synthesizing the source code into a gate-level netlist including at least one instrumentation signal, wherein the instrumentation signal is indicative of an execution status of the at least one statement.

Applicant respectfully asserts that whereas amended claim 1 refers to operating on "register transfer level (RTL) synthesizable source code", Chen et al., in contrast, is directed to the operation on an analyzable HLS, or High Level Synthesis, design (Chen, page 137, §3. Design annotation, first paragraph, first sentence). High Level Synthesis designs are not designs that are synthesizable by logic synthesis tools. Moreover, claim 1 includes "synthesizing the source code into a gate-level netlist including at least one instrumentation signal". In contrast, Chen et al. teaches away from the application of design annotations, such as instrumentation signals, to gate level designs due to the overhead that would be incurred in downstream synthesis tools (Chen, page 137, §3.Design annotation, second paragraph, first sentence).

Therefore, Applicants respectfully submit that for at least the reasons stated above, amended claim 1 is not anticipated by Chen et al. and should therefore be allowed.

Given that claims 5, 12, 16, 20, 30 and 32, as amended, include substantially equivalent elements to that of claim 1, Applicants respectfully submit that claims 5, 12, 16, 20, 30 and 32 are similarly not anticipated by Chen et al. for at least the reasons discussed above and should therefore be allowed.

Given that claims 2-4, 6-11, 13-14, 17-18, 22-23, 31 and 33 depend from allowable claims 1, 5, 12, 16, 20, 30 and 32 respectively, and dependent claims necessarily include all the elements of the claim from which they depend, Applicants respectfully submit that, claims 2-4, 6-11, 13-14, 17-18, 22-23, 31 and 33 are not anticipated by Chen et al. for at least the reasons discussed above and should therefore be allowed.

Claims 24-25

In the February 01, 2000 Office Action, claim 24 was rejected as being unpatentable over a reference to Chen et al. In response, Applicant respectfully disagrees.

Claim 24 includes:

> A method of simulating a gate-level design comprising the steps of:
>
> a) identifying a sensitivity list of a process;
>
> b) generating logic to identify signal events for any signal in the sensitivity list; and
>
> c) identifying the process as active during simulation when a signal event occurs for any signal in the sensitivity list.

In claim 24 a process is identified as being active by **logic** that was generated to identify signal events. The Chen et al reference, on page 137, column 1, third paragraph, and figure 2 describes a value change database. Arguably this database,

through manipulation, could be used to determine if a process is active. However this would not be done via **generated logic**. Therefore, Chen et al. does not suggest, disclose, or enable "generating logic to identify signal events" as claimed in claim 24.

Thus, Applicants respectfully submit that for at least the reasons stated above, claims 24 is not anticipated by Chen et al. and should therefore be allowed.

Given that claim 25 depends from allowable claim 24 and dependent claims necessarily include all the limitations of the claim from which they depend, Applicants respectfully submit that claim 25 is not anticipated by Chen et al. for at least the reasons stated above and should therefore be allowed.

35 U.S.C. §103

In the February 01, 2000 Office Action, claims 15, 19, 21, 26 and 27 were rejected under 35 U.S.C. § 103 as being unpatentable over Chen et al. in view Koch et al ("Debugging of Behavioral VHDL Specification by Source Level Emulation", Proceedings of the European Design Automation Conference, pp. 256-261, September 1995, hereinafter "Koch"). Given that claims 15, 19, 21, 26 and 27 depend from 12, 16, 20, and 24, the reasoning above applies with respect to Chen et al. Applicant respectfully submits that Koch et al. does not cure the deficiency of Chen et al. as discussed above. Therefore, for at least the same reasons as those discussed above, the applicant submits that these claims should be allowed.

In conclusion, Applicant respectfully submits that claims 1-33 are in a condition for allowance, and Applicant respectfully requests allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 02-2666.

Respectfully submitted,

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